UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,355	07/10/2003	Norikatsu Takaura	XA-9689A	1568

181 7590 11/17/2004

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,355	TAKAURA ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-13 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-13 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 10 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/164,008.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/10/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 6, 8, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,251,721 to Kanazawa et al. in view of U.S. Patent No. 6,424,016 to Houston.

Regarding claim 1, Kanazawa discloses a production method for an IC device having a memory cell selecting n-MISFET (transistors in 107; see figure 7c) and a capacitor (171; see figure 12) formed in a memory cell area (107) and an n-MISFET (transistor in well 111 of region 108; see figure 7c) and a p-MISFET (transistor in well 112 in region 108) in the peripheral circuit area (108), comprising: a step of forming a gate insulating film (105) on the substrate (figure 7b); a gate electrode forming step of forming a silicon film (113) and an insulating film (116,117) on the gate insulating film (figure 7c), and forming, by patterning, gate electrodes for the MISFETs (figures 7c, 8a), where the gate electrodes include dopants (column 10, lines 17-18); sequentially depositing a first (122) and a second (123) film on the substrate, and leaving, by anisotropically etching, the films on a sidewall of the gate electrodes in the peripheral region (figure 8b; column 10, lines 45- 50) and filling the spaces between the gate electrodes in the memory cell area with the films (figure 8a, 8b); and using the films as a mask to implant an impurity into both sides of the peripheral MISFETs (figures 8b, 8c; column 10, lines 52-58).

Kanazawa merely teaches that the gate electrode material is doped (see column 10, line 17), but fails to specify the doping type of each of the gate electrodes in the memory and peripheral regions.

Houston teaches that for a DRAM structure (which is substantially similar to that disclosed by Kanazawa), it is advantageous to use p-doped gates with an n-MISFET or n-doped gates with a p-MISFET for the memory cell pass transistors, and use either type of dopant for the gate electrodes of the peripheral transistors (see column 1, lines 35- 62; column 3, lines 10-22; column 4, lines 55-67; column 5, lines 12-25; and column 6, lines 15-40).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify in the DRAM process of Kanazawa that the memory n-MISFET and peripheral p-MISFET have p-type gates, and the peripheral n-MISFET has an n-type gate, as suggested by Houston. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a p-doped gate for the memory cell n-MISFET, because doing so raises the threshold voltage of the memory transistor, which in turn, reduces the leakage of the gate (see Houston, column 1, lines 35-62; column 4, lines 55-67). A person skilled in the art would further have used n-doped gates with the n-MISFETs and p-doped gates with the p-MISFETs in the peripheral circuit, because Houston shows that such an arrangement allows for optimal performance of the peripheral transistors (see column 5, lines 10-17; column 6, lines 15-30).

Regarding claim 2, Kanazawa discloses removing the second film and then the first film in the memory cell forming area (figures 9b, 10b); and filling, with a conductive film, the space between the gate electrodes of the memory cell (figures 9c, 11a).

Regarding claims 6, 8, and 9, Kanazawa discloses that the insulating film and first film are SiN (column 10, lines 18-20, and 37-39), which is intrinsically a barrier against hydrogen penetration. Kanazawa further teaches that the second film is a silicon oxide film (column 10, lines 38-40), which has different etching selective ratios to SiN.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa et al. in view of Houston, as applied to claim 2 above, and further in view of U.S. Patent No. 5,946,548 to Hashimoto et al.

Kanazawa fails to disclose a step of polishing the conductive film on the gate electrodes until the first film on the gate electrode is exposed.

Hashimoto discloses a DRAM structure in which the conductive contact film (22) is disposed over the entire structure, and then polished by CMP until the first film (20) on the gate electrode is exposed (see figures 12-13).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Kanazawa as modified by Houston, that the conductive film is planarized to expose the first film on the gate electrodes, as suggested by Hashimoto. The rationale is as follows: A person having ordinary skill in the art would have been motivated to planarize the conductive film and expose the first film, because doing so flattens the entire device surface at a controllable thickness over the gate electrodes (see Hashimoto, column 7, lines 1-36), which in turn allows for a more controlled and even disposition of overlying layers, better resolution for subsequent photolithographic processes, and better control of the circuit design, as is appreciated by one skilled in the art.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa et al. in view of Houston and U.S. Patent No. 5,866,460 to Akram et al.

Kanazawa discloses a production method for an IC device having a memory cell selecting n-MISFET (transistors in 107; see figure 7c) and a capacitor (171; see figure 12) formed in a memory cell area (107) and an n-MISFET (transistor in well 111 of region 108; see figure 7c) and a p-MISFET (transistor in well 112 in region 108) in the peripheral circuit area (108), comprising: a step of forming a gate insulating film (105) on the substrate (figure 7b); a gate electrode forming step of forming a silicon film (113) and an insulating film (116) on the gate insulating film (figure 7c), and forming, by patterning, gate electrodes for the MISFETs (figures 7c, 8a), where the gate electrodes include dopants (column 10, lines 17-18); using, as a mask, the gate electrode of the memory cell and the capping film to implant an impurity into both sides of the gate electrode (figure 7c; column 10, lines 30-35) as well as implanting the n-MISFET and p-MISFET in the peripheral region (figure 7c); sequentially depositing a first (122) and a second (123) film on the substrate, and leaving, by anisotropically etching, the films on a sidewall of the gate electrodes in the peripheral region (figure 8b; column 10, lines 45- 50) and filling the spaces between the gate electrodes in the memory cell area with the films (figure 8a, 8b); and using the films as a mask to implant an impurity having a higher concentration than the previously implanted impurity into both sides of the peripheral MISFETs (figures 8b, 8c; column 10, lines 52-58).

Kanazawa merely teaches that the gate electrode material is doped (see column 10, line 17), but fails to specify the doping type of each of the gate electrodes in the memory and

peripheral regions. Kanazawa further fails to teach that the implant aligned with the sidewalls in the peripheral region occurs before the implant aligned with the gates in the peripheral region.

Houston teaches that for a DRAM structure (which is substantially similar to that disclosed by Kanazawa), it is advantageous to use p-doped gates with an n-MISFET or n-doped gates with a p-MISFET for the memory cell pass transistors, and use either type of dopant for the gate electrodes of the peripheral transistors (see column 1, lines 35- 62; column 3, lines 10-22; column 4, lines 55-67; column 5, lines 12-25; and column 6, lines 15-40).

Akram teaches that an impurity region similar to that of Kanazawa can be formed either by implanting aligned with the gate, and then implanting aligned with a sidewall (see figures 1A-1D), or by implanting aligned with the sidewalls, removing the sidewalls, and then implanting aligned with the gate (see figures 2A-2D).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify in the DRAM process of Kanazawa that the memory n-MISFET and peripheral p-MISFET have p-type gates, and the peripheral n-MISFET has an n-type gate, as suggested by Houston, and such that the sidewall-aligned implant in the peripheral region occurs before the gate-aligned implant, as suggested by Akram. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a p-doped gate for the memory cell n-MISFET, because doing so raises the threshold voltage of the memory transistor, which in turn, reduces the leakage of the gate (see Houston, column 1, lines 35-62; column 4, lines 55-67). A person skilled in the art would further have used n-doped gates with the n-MISFETs and p-doped gates with the p-MISFETs in the peripheral circuit, because Houston shows that such an arrangement allows for optimal performance of the peripheral transistors (see

column 5, lines 10-17; column 6, lines 15-30). A person having ordinary skill in the art would further have been motivated to change the order of the peripheral implants, because Akram shows that both methods are known alternate means for forming a multiple-implant source or drain region (see Akram, column 7, lines 20-45).

5. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa et al. in view of Houston and U.S. Patent No. 6,153,476 to Inaba et al.

Kanazawa discloses a production method for an IC device having a memory cell selecting n-MISFET (transistors in 107; see figure 7c) and a capacitor (171; see figure 12) formed in a memory cell area (107) and an n-MISFET (transistor in well 111 of region 108; see figure 7c) and a p-MISFET (transistor in well 112 in region 108) in the peripheral circuit area (108), comprising: a step of forming a gate insulating film (105) on the substrate (figure 7b); a gate electrode forming step of forming a silicon film (113) and an insulating film (116) on the gate insulating film (figure 7c), and forming, by patterning, gate electrodes for the MISFETs (figures 7c, 8a), where the gate electrodes include dopants (column 10, lines 17-18); sequentially depositing a first (122) and a second (123) film on the substrate, and leaving, by anisotropically etching, the films on a sidewall of the gate electrodes in the peripheral region (figure 8b; column 10, lines 45- 50) and filling the spaces between the gate electrodes in the memory cell area with the films (figure 8a, 8b); and using the films as a mask to implant an impurity into both sides of the peripheral MISFETs (figures 8b, 8c; column 10, lines 52-58).

Kanazawa merely teaches that the gate electrode material is doped (see column 10, line 17), but fails to specify the doping type of each of the gate electrodes in the memory and

peripheral regions. Kanazawa further fails to teach removing the first film from the semiconductor substrate in the memory area between the steps of depositing the film and depositing the second film.

Houston teaches that for a DRAM structure (which is substantially similar to that disclosed by Kanazawa), it is advantageous to use p-doped gates with an n-MISFET or n-doped gates with a p-MISFET for the memory cell pass transistors, and use either type of dopant for the gate electrodes of the peripheral transistors (see column 1, lines 35- 62; column 3, lines 10-22; column 4, lines 55-67; column 5, lines 12-25; and column 6, lines 15-40).

Inaba discloses a method substantially similar to that of Kanazawa, except that the first film is removed from the substrate immediately after deposition (see figure 2B).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify in the DRAM process of Kanazawa that the memory n-MISFET and peripheral p-MISFET have p-type gates, and the peripheral n-MISFET has an n-type gate, as suggested by Houston, and further that the first film is removed from the substrate, as taught by Inaba. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a p-doped gate for the memory cell n-MISFET, because doing so raises the threshold voltage of the memory transistor, which in turn, reduces the leakage of the gate (see Houston, column 1, lines 35-62; column 4, lines 55-67). A person skilled in the art would further have used n-doped gates with the n-MISFETs and p-doped gates with the p-MISFETs in the peripheral circuit, because Houston shows that such an arrangement allows for optimal performance of the peripheral transistors (see column 5, lines 10-17; column 6, lines 15-30). A person skilled in the art would have been further motivated to remove the first film from the

substrate in the memory cell area, in order to simplify the contact hole etching step. Since the first and second films have a large etching rate difference (see Inaba, column 8, lines 1-20 and lines 40-60), two separate etching steps would have been required to remove the first and second films in the contact hole. By combining the step of removing portions of the first layer in the memory are with the isotropic, sidewall spacer etch in the peripheral area, one etching process step is eliminated from the process, as is appreciated by one skilled in the art.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa et al. in view of Houston, as applied to claim 1 above, and further in view of U.S. Patent No. 6,383,921 to Chan et al.

Kanazawa fails to teach that the first and second films are silicon oxide and silicon, respectively.

Chan teaches that for forming a self-aligned contact structure to a source/drain region, it is advantageous to use sidewall films of silicon oxide and polysilicon (see column 2, lines 1 – 25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the first and second films of Kanazawa as modified by Houston, such that they are SiO and poly-Si, as suggested by Chan. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use a SiO/poly-Si gate sidewall stack, because Chan shows that the poly-Si and the SiO have extremely high etching selectivity, which allows for increased protection of the gate electrode during contact hole formation (Chan, column 2, lines 13-25).

7. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa as modified by Houston and Inaba, as applied to claim 10 above, and further in view of U.S. Patent No. 6,440,495 to Wade et al.

Kanazawa fails to teach that the capacitor plates are metal, with at least one plate made of ruthenium.

Wade teaches that ruthenium is a preferred material for DRAM capacitor plates (column 1, lines 15-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the process of Kanazawa as modified by Houston and Inaba, such that the capacitor plates are made of Ru, as suggested by Wade. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use ruthenium for the capacitor plates, because it is compatible with many high dielectric constant insulators, thus increasing the storage capacity, has a low resistivity, and has good thermal properties, as is well known by a person having ordinary skill in the DRAM arts (also, see Wade, column 1, lines 15-27).

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazawa et al. in view of Houston, as applied to claim 1 above, and further in view of U.S. Patent No. 5,629,887 to Nakano et al.

Kanazawa is silent as to whether the arrangement is an open-bit-line.

Nakano teaches that DRAMs can be formed in an open bit line arrangement (column 1, lines 25-35).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the method of Kanazawa as modified by Houston uses an open bit line arrangement, as suggested by Nakano. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use an open bit line arrangement, because doing so maximizes the density of the memory cells, which in turn reduces the chip area (see Nakano, column 1, lines 25-35).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813
jmd

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800